



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/084,652   | 02/28/2002  | Timothy D. Wilkinson | 124-930             | 3971             |
| 23117  | 7590        | 12/13/2005           | EXAMINER            |                  |
| NIXON & VANDERHYE, PC<br>901 NORTH GLEBE ROAD, 11TH FLOOR<br>ARLINGTON, VA 22203 |             |                      | PHAN, THANH S       |                  |
|  |             |                      | ART UNIT            | PAPER NUMBER     |
|  |             |                      | 2841                |                  |

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/084,652

Applicant(s)

WILKINSON ET AL.

Examiner

Thanh S. Phan

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 and 28-34 is/are rejected.
- 7) ☒ Claim(s) 22-27 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

Applicant's argument dated 08/05/05 is persuasive. The application is hereby reopened prosecution in light of the newly found prior arts.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-21 and 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akinwande et al. [US 5,646,702] in view of Kajita et al. [US 6,275,280].

Regarding claim 1, Akinwande et al. disclose a backplane [substrate 71] comprising an array [100] of electrical or electronic elements [fig 19], each of said electrical or electronic elements comprising at least a first and second electronic element layers [84, 98] and at least one spacer [99] which rises higher over the back plane and the array.

Akinwande et al. disclose the claimed invention except for the spacer comprising a first layer and a second layer being of **substantially** the same material as the electronic layers.

Kajita et al. disclose an LCD device with spacers having a first and second layer [figs 1 and 3-5] and further teaches that different material can be used [column 8, lines 43+].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the spacer design of Kajita et al. with Akinwande et al.'s for the purpose of having sufficient load compression displacement and light screening requirement.

Regarding claim 2, Akinwande et al. disclose wherein the backplane is a semiconductor backplane [backplane 71 provides conductivity for the mounted components].

Regarding claim 3, Akinwande and Kajita et al. disclose [see claim 1] wherein the at least one spacer includes at least one additional space layers, said at least one additional spacer layer and said first and second spacer layers forming a series of more than two layers.

Regarding claim 4, Akinwande et al. disclose a backplane [substrate 71] comprising an array [100] of electrical or electronic elements [fig 19], each of said electrical or electronic elements comprising at least a first and second electronic element layers [84, 98] and at least one spacer [99] which rises higher over the back plane and the array.

Akinwande et al. disclose the claimed invention except for the spacer comprising a first layer and a second layer, wherein the material of said first spacer layer is **modified relatively** to the material of said first electronic element layer.

Kajita et al. disclose an LCD device with spacers having a first and second layer [figs 1 and 3-5] and further teaches that different material can be used [column 8, lines 43+].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the spacer design of Kajita et al. with Akinwande et al.'s for the purpose of having sufficient load compression displacement and light screening requirement.

Regarding claim 5, Akinwande et al. disclose the claimed invention except for wherein all the layers in the spacer corresponding in material and order to all the layers in said at least one electrical or electronic element.

Kajita et al. disclose an LCD device with spacers having a first and second layer [figs 1 and 3-5] and further teaches that different material can be used [column 8, lines 43+].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the spacer design of Kajita et al. with Akinwande et al.'s for the purpose of having sufficient load compression displacement and light screening requirement.

Regarding claim 6, Akinwande et al. disclose wherein the spacer is electrically insulating [dielectric] between a top and bottom of said spacer.

Regarding claims 7 and 8, Akinwande et al. disclose the claimed invention except for wherein a plurality of spacers regularly distributed.

Kajita et al. disclose a plurality of spacers regularly distributed over a backplane [figs 1 and 3-5].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a plurality of spacers distributed over a backplane for the purpose of supporting one substrate over another.

Regarding claims 9 and 10, Akinwande et al. disclose the claimed invention except for wherein the array providing a plurality of addressable locations with each location having a spacer associated therewith.

Kajita et al. discloses the array providing a plurality of addressable locations with each location having a spacer associated therewith [fig 6].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the array providing a plurality of addressable locations with each location having a spacer associated therewith to provide adequate supports of the LCD device.

Regarding claims 11-12, Akinwande et al. disclose the claimed invention except for wherein the spacers comprise different shapes.

Kajita et al. disclose wherein the spacers comprise different shapes [figs 3-4].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a specific shape(s) and/or size(s) as suggested by Kajita et al. with Akinwande et al. for the purpose of providing a corresponding arrangement of element within a particular backplane configuration.

Regarding claims 13-15, Akinwande et al. disclose an insulating layer [96] having a general constant thickness extending over at least one layer.

Regarding claims 16-20 and 32-34, Akinwande et al. disclose a reflective layer [glass screen 95] mounted on the insulating layer.

Regarding claim 21, Akinwande et al. disclose wherein a spacer [99] is located outside of the array.

Regarding claims 28-31, the claimed method steps are necessitated by the product structures since the apparatus structures are disclosed by Akinwande et al., as modified.

#### ***Allowable Subject Matter***

Claims 22-27 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Response to Arguments***

Applicant's arguments with respect to claims 1-21 and 28-34 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Saito et al [US 6,373,547]; Wysocki et al. [US 5,111,320] ; Krusius et al. [US 6,476,886] ; Chen et al. [US 6,521,475].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh S. Phan whose telephone number is 571-272-2109. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tsp



**KAMAND CUNEO**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**